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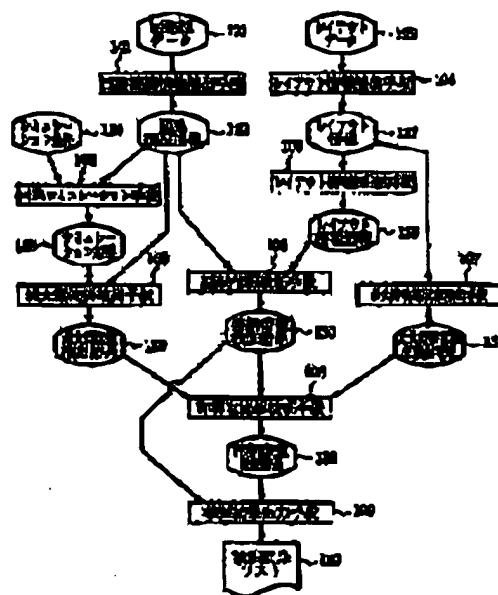
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(54) LAYOUT VERIFICATION SYSTEM

(57)Abstract:

PURPOSE: To provide a layout verification system which can precisely verify a layout without using a manual processing.

CONSTITUTION: A circuit connection information extraction means 101, a circuit simulation means 102, a maximum current extraction means 103, a layout information extraction means 104, a layout connection information extraction means 105, a connection information verification means 106, a maximum allowance current value extraction means 107, an allowance current value verification means 108 and a verification result output means 109 are provided. A maximum current value extraction result 129 flowing in respective elements on circuit drawing data obtained by the maximum current value extraction means 103 and a maximum allowance current value extraction result 131 flowing in the respective wirings and elements, which are constituted on layout data obtained by the maximum allowance current value extraction means 107, are compared and referred to by the allowance current value verification means 108 through a connection information verification result 130 outputted from the connection information verification means 106.



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